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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/021,388	12/06/2001	Dean A. Klein	MTIPAT.073DV1	3167

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EXAMINER	
DINH, SON T	

ART UNIT	PAPER NUMBER
2824	

DATE MAILED: 05/12/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/021,388	KLEIN, DEAN A.	
	Examiner	Art Unit	
	son t dinh	2824	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on 2/2/04 .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-11 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-11 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 06 December 2001 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☑ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☒ Other: *East search history* .

DETAILED ACTION

The RCE and the amendment A filed on 2/2/04 have been entered.

Claims 1-11 are pending in the application.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

Claims 2-7, 9-11 are rejected under 35 U.S.C. 102(e) as being anticipated by Iwamoto et al (U.S. Patent No 5,764,590).

For the purpose of this rejection, an input/output terminal would be considered as a contact (as defined by the applicant), and a selector would be considered as a

parasitic capacitance control bus switch because this selector performs the function of connecting and disconnecting (enabling and disabling) a data bus from an input buffer. Note that there is no particular definition for parasitic capacitance control switch in the electrical field, then any switch (or device that can connects and disconnects between a bus) that connects between a bus and perform the function of connecting and disconnecting the bus would be considered as a parasitic capacitance control switch.

Regarding claims 2-3, figure 9 (also see figure 11 for more detail) of Iwamoto et al discloses a memory device comprising a contact (112, 113) connects to a data bus (the bus that connected 112 or 113 to the switch 904 (selector)), a parasitic capacitance control switch (904) having input connected to the contact 112 (or 113) and an output connected to an input buffer (905a, 905b). See column 12, lines 4-15.

Regarding claims 4-5, 7, element 501 (figure 5) is one control terminal, and 502 (figure 5) is a logic circuit that is configured to selectively open the parasistic capacitance control switch 904 (figure 11). Also, elements 1101 and 1102 in figure 11 would be a control portion as claimed in claim 5.

Regarding claim 6, the circuit 103 in figure 10B of Iwamoto et al has one control terminal (ext/WE) for receiving memory access control signal (WE) and coupled to the control terminal 501.

Regarding claims 9-10, the parasitic capacitance control switch 904 is a transfer gate and when input buffer 905a is not selected (no access is occurring), then the step of disabling is performed, and when input buffer a is selected (access is occurring), then

the step of enabling is performed. The step of transferring data in claim 10 is performed by switch 904 (or transfer gate 904).

Regarding claim 11, for the purpose of this rejection, means for enabling and means for disabling would be considered as a single means that could perform both functions (see the 112 rejection above). Then switch 904 would be means for performing the function of enabling a transfer gate when there is an access, and disabling when there is no access. See the rejection applied to claims 9-10 for the access of the memory and the operation of the switch.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1 and 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Iwamoto et al in view of Miyai et al (U.S. Patent No 5,537,584).

Iwamoto et al applied as above. The only difference between Iwamoto et al and claim 8 is that Iwamoto et al is silent on the use of circuit or a state decoder for generating a chip select signal. Miyai et al teaches that the use of a circuit (22 figure 8) for generating a chip select signal so as to enable the operation of the integrated circuit is well known in the art. The element 22 of Miyai et al would be considered as a state decoder since this circuit could perform the function of generating a chip select signal.

Therefore, it would have been obvious to one ordinary skill in the art at the time the invention was made to modify Iwamoto et al by using a state decoder for generating a chip select signal which is applied to the integrated circuit so as to enable the operation of the integrated circuit as evidenced by Miyai et al.

Response to Arguments

The applicant argues that the selector of Iwamoto et al is not used for the purpose of controlling the parasitic capacitance of a bus. The Examiner disagrees. It is noted that the selector of Iwamoto et al function as a switch (connecting or disconnecting the bus from an input buffer), and such selector would perform the function of electrically isolating portions of a bus, then the selector inherently controls the parasitic capacitance on the bus. Note that the applicant agrees that by electrically isolating portions of a bus, the parasitic capacitance would be control. Specifically, when signal B8E is at high level (H), /B8E is at low level (L), the signal at contact 113 is not applied to 905B, i.e. the element 1102 (figure 11) clearly isolates the portion from the input of 1102 to 113, and the portion between the output of 1102 and input buffer 905b. The Examiner agrees with the applicant that the selector 904 performing the function of routing information. However, this selector (904) also performs the function of isolating a portion of a data bus as explained above.

The applicant also argues that Miyai fails to teach the use of a chip select signal so as to control the parasitic capacitance of a bus. Note that claims 1 and 8 state that the switch is used for the purpose of controlling the parasitic capacitance of a bus, not

the chip select signal itself. It is also noted that the amended claims 1 and 8 only recited that the switch is used to control the parasitic capacitance (not the chip select signal), and in the remark (page 2, third paragraph), the applicant argues that the applied art fail to show the chip select signal to control parasitic capacitance. It is not directed to the ground of the rejection.

Therefore, the applicant arguments are not persuasive for the reasons stated above.

Conclusion.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Son t Dinh whose telephone number is 571-272-1868. The examiner can normally be reached on 8am-5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Elms can be reached on 571-272-1869. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7724 for regular communications and 703-308-7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

S. Dinh
May 1th, 2004

Son T. Dinh
Primary Examiner